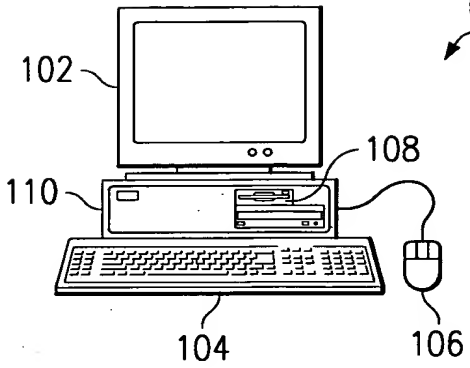
#3

FIG. 1



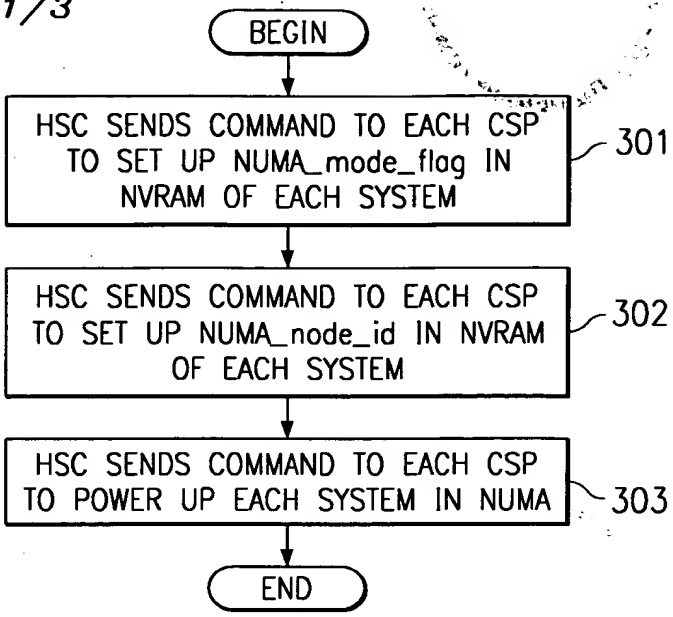


FIG. 3

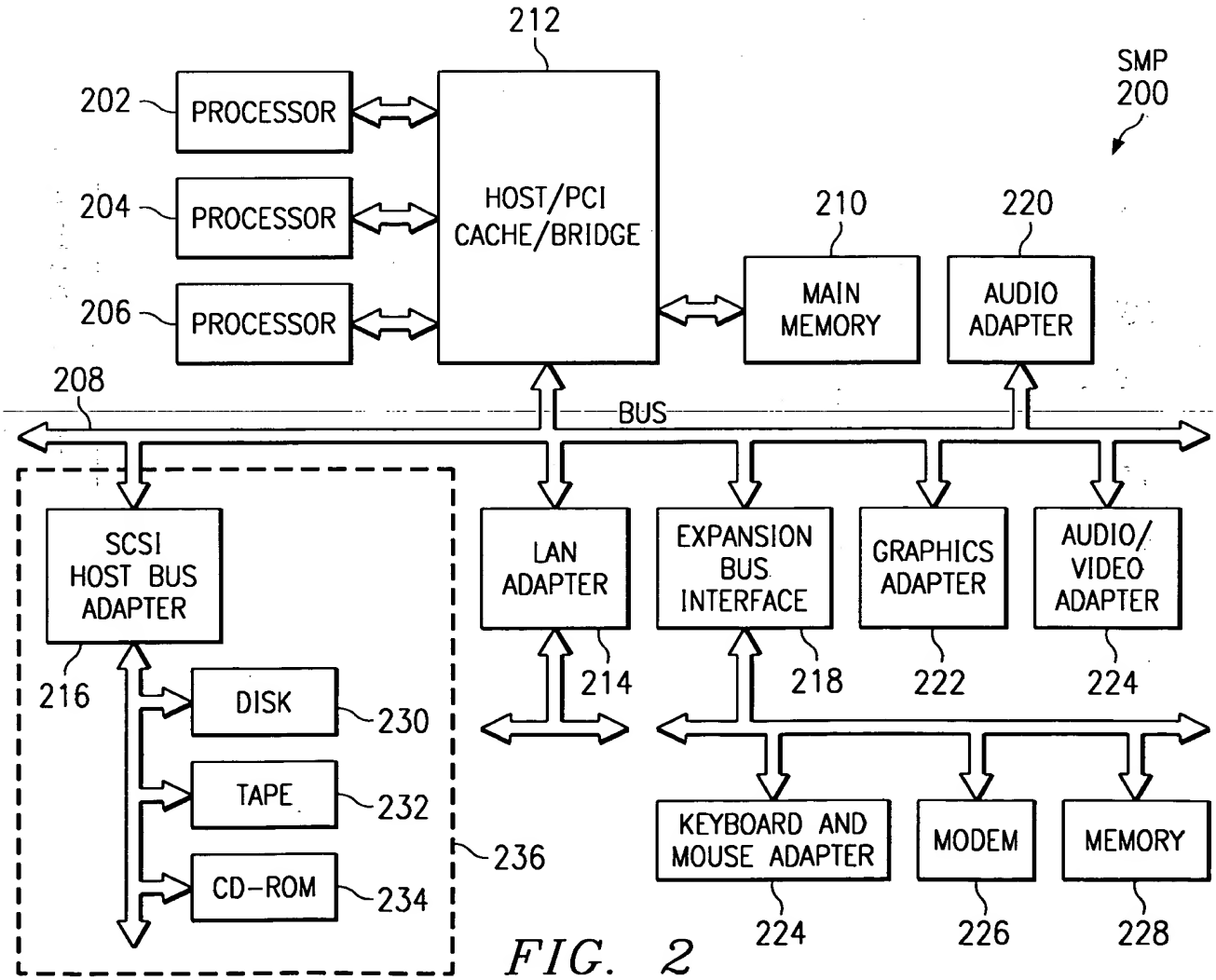


FIG. 2

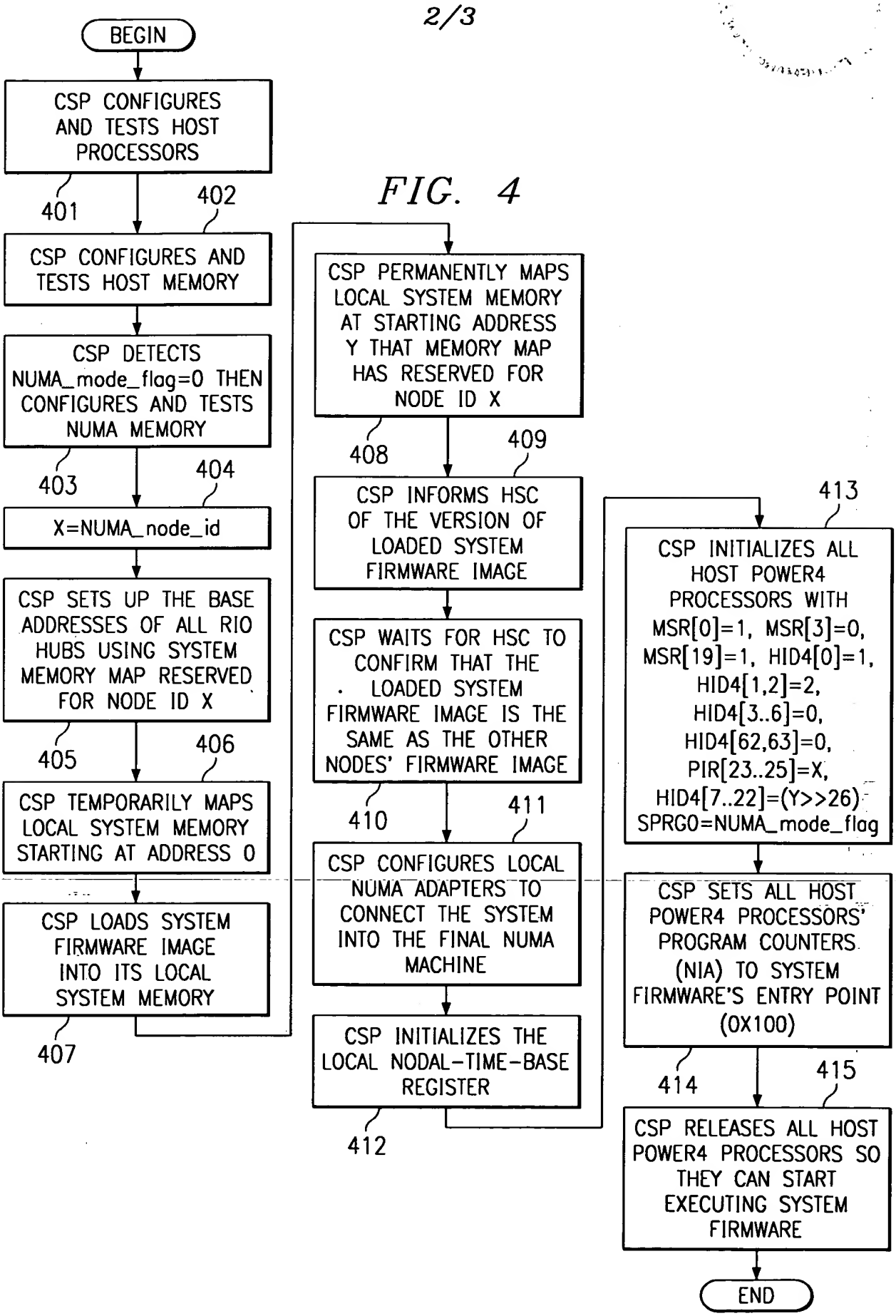

BEGIN
CSP CONFIGURES AND TESTS HOST PROCESSORS
401
CSP CONFIGURES AND TESTS HOST MEMORY
402
CSP DETECTS NUMA_mode_flag=0 THEN CONFIGURES AND TESTS NUMA MEMORY
403
X=NUMA_node_id
404
CSP SETS UP THE BASE ADDRESSES OF ALL RIO HUBS USING SYSTEM MEMORY MAP RESERVED FOR NODE ID X
405
CSP TEMPORARILY MAPS LOCAL SYSTEM MEMORY STARTING AT ADDRESS 0
406
CSP LOADS SYSTEM FIRMWARE IMAGE INTO ITS LOCAL SYSTEM MEMORY
407
CSP PERMANENTLY MAPS LOCAL SYSTEM MEMORY AT STARTING ADDRESS Y THAT MEMORY MAP HAS RESERVED FOR NODE ID X
408
CSP INFORMS HSC OF THE VERSION OF LOADED SYSTEM FIRMWARE IMAGE
409
CSP WAITS FOR HSC TO CONFIRM THAT THE LOADED SYSTEM FIRMWARE IMAGE IS THE SAME AS THE OTHER NODES' FIRMWARE IMAGE
410
CSP CONFIGURES LOCAL NUMA ADAPTERS TO CONNECT THE SYSTEM INTO THE FINAL NUMA MACHINE
411
CSP INITIALIZES THE LOCAL NODAL-TIME-BASE REGISTER
412
CSP INITIALIZES ALL HOST POWER4 PROCESSORS WITH MSR[0]=1, MSR[3]=0, MSR[19]=1, HID4[0]=1, HID4[1,2]=2, HID4[3..6]=0, HID4[62,63]=0, PIR[23..25]=X, HID4[7..22]=(Y>>26) SPRG0=NUMA_mode_flag
413
CSP SETS ALL HOST POWER4 PROCESSORS' PROGRAM COUNTERS (NIA) TO SYSTEM FIRMWARE'S ENTRY POINT (0X100)
414
CSP RELEASES ALL HOST POWER4 PROCESSORS SO THEY CAN START EXECUTING SYSTEM FIRMWARE
415
END

FIG. 4

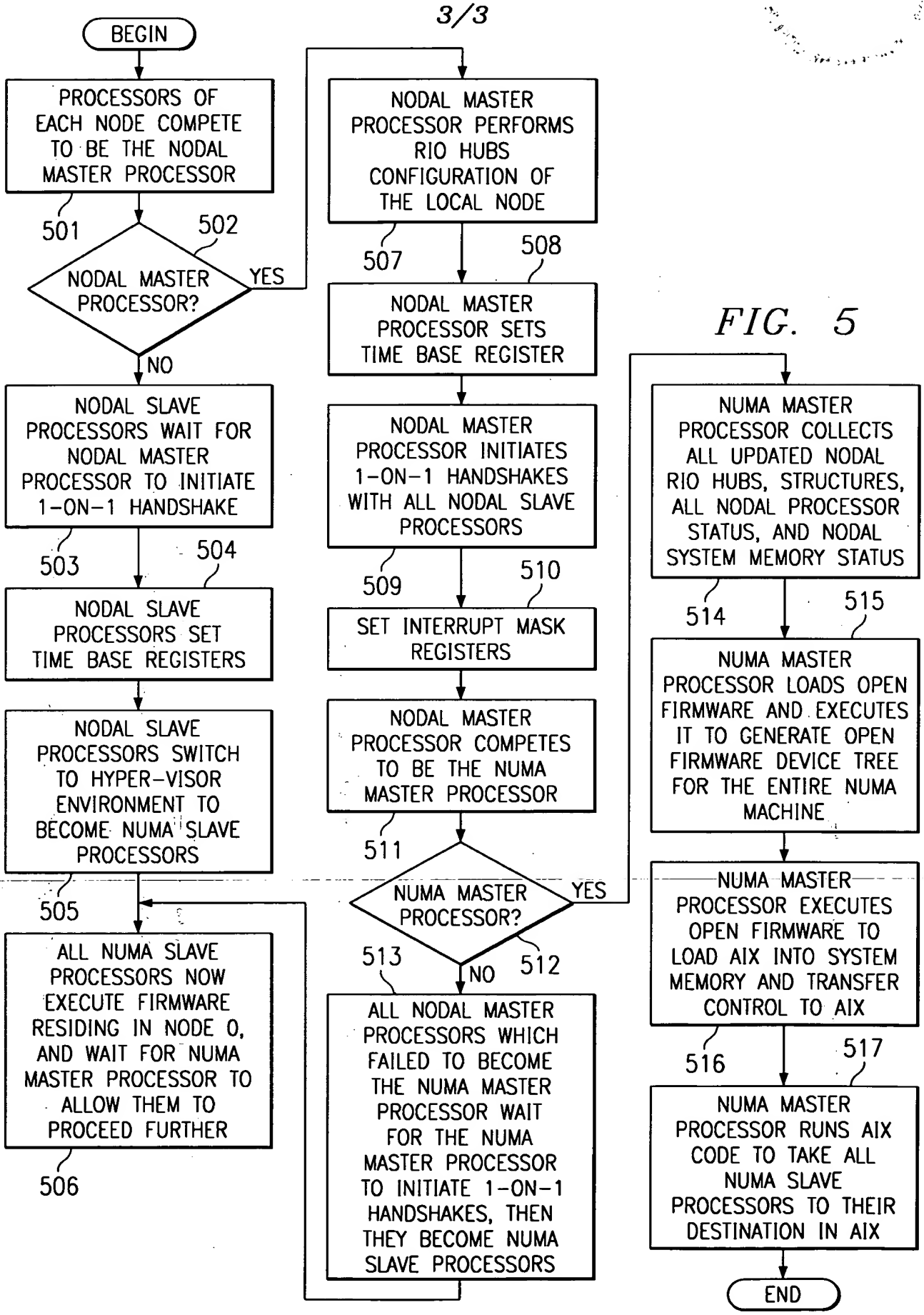


FIG. 5

Patent Application Publication